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Please find below and/or attached an Office communication concerning this application or proceeding.

09/537669

1. Claims 11 & 12 should be included in the Rejection statement on page 5. Claim 9 should not be included.
Claim 15 should be included in the Rejection statement on p. 9

2. Claim 1 - How is the cited portion of Levine interpreted to control a "image data"? (Row of)

3. Claim 1 - How does col. 2, lines 15-16 of Levine Teach "pixels adjacent ---"?

4. In general - why isn't Pape a "102" on this claim? (Claim 1)
1st field = storing the image data at a "first time"
2nd field = storing the defect data at a "second time"
(Pape has to not only write image data into the memory, it inherently also must read the image data out of the memory in order to provide an image to be viewed/processed.)
The other features of claim 1 seem (at first glance) to also be in Pape.

5. Claim 2 - Can Pape also read on this (102)?
The image data at pixel(X,Y) seems to be for the previously recorded noise data at the same x,y location. (col. 4, lines 35-36).

~~Claim 3 - How does Rambaldi teach the limitation "consecutive defective pixels"?~~

Claim 16 - would dividing by 2 be the same as cutting a lowest one bit (2')?
If so this would be obvious.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pape et al. (US Patent # 5,047,863) in view of Levine (US Patent No. 4,600,946).

Re claim 1, Pape discloses "an image processing apparatus for processing image data supplied from an image sensor, comprising:

a) "a memory having a first field for storing image data of one frame and a second field for storing position data of a defective pixel of the image sensor;" (Pape col. 3 lines 43-49).

However Pape fails to disclose the following:

b) "control means for controlling image data to write into said memory and image data to read from said memory; (Levine, col. 6 lines 32-45 figure 3)[ROM logic 304 in figure 3 acts as a control means].

c) "a counter for counting the number of pixels of image data sequentially transferred from the image sensor;" (Levine, col. 6 lines 56-59 figure 3)

d) "and a defect correction circuit for correcting the image data of each pixel sequentially transferred from the image sensor in accordance with image data of pixels adjacent to a pixel whose image data is currently transferred (Levine, col. 2 lines 15-18).

e) "wherein said control means writes the image data corrected by said defect correction circuit in the first field of said memory at a storage location corresponding to the defect pixel, if a count of said counter becomes coincident with a number corresponding to the position data of the defective pixel in the second field of said memory, and writes the image data supplied directly from the image sensor in the first field, if the count is not coincident with the number corresponding to the position data of the defective pixel" (Levine col. 6 lines 45-55).)[ROM logic 304 in figure 3 acts as a control means].

However the above limitations are well known in the art as evidenced by Levine for example limitation b) (col. 6 lines 32-45 figure 3)[ROM logic 304 in figure 3 acts as a control means],

c) (col. 6 lines 56-59 figure 3),

d) (col. 2 lines 15-18)

e) (col. 6 lines 45-55).)[ROM logic 304 in figure 3 acts as a control means].

Therefore taking the combined teachings of Pape and Levine as a whole, it would have been obvious to one skilled in the art to incorporate b,c,d and e. Doing so would provide a higher yield of usable broadcast quality imagers thereby reducing the cost per imager as suggested by Levine (col. 2 lines 10-12).

Claim 10 is a method claim corresponding to the apparatus claim 1. Therefore it has been analyzed and rejected based on the claim 1.

3. Claims 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pape et al. (US Patent # 5,047,863) in view of Levine (US Patent No. 4,600,946) in further view of Fossum(US Patent # 6611288)

Re claim 2, Pape and Levine fail to teach "An image processing apparatus according to claim 1, wherein a storage location in said memory is identified by a row address and a column address, the first field stores the image data of each line at a corresponding row address, and the second field stores the position data of the defective pixel at the same row address". However the above limitations are well known in the art as evidenced by Fossum (col. 3 lines 52-65)[Lines 52-54 indicate the storage location in terms of row address and a column address. It further describes how a "T" bit To indicates a bad row, column or a single defective pixel. If none of the pixels is dead in a row or a column then that row is not flagged. So we can infer that the memory storage has image data stored in the row address and a second field stores the position of the defective pixel i.e. the bit To.]

Therefore taking the combined teachings of Pape, Levine and Fossum as a whole, it would have been obvious to one skilled in the art to incorporate a storage location in said memory identified by a row address and a column address, the first field stores the image data of each line at a corresponding row address, and the second field stores the position data of the defective pixel at the same row address. Doing so facilitates substitution using the nearest neighbor technique as evidenced in Fossum (col. 3 lines 66-67).

4. Claims 3/1,4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pape et al. (US Patent # 5,047,863) in view of Levine (US Patent No. 4,600,946) in further view of Rambaldi et al. (US Patent # 6618084).

Re claim 3/1, Pape and Levine fail to teach "An image processing apparatus according to claim 1, wherein the second field of said memory stores information representative of a single defective pixel or the number of consecutive defective pixels and information representative of a position of the defective pixel in each line". However the above limitations are well known in the art as evidenced by Rambaldi (col. 3 lines 35-38, 49-50).

Therefore taking the combined teachings of Pape, Levine and Rambaldi as a whole, it would have been obvious to one skilled in the art to incorporate second field of said memory storing information representative of a single defective pixel or the number of consecutive defective pixels and information representative of a position of the defective pixel in each line. Doing so would recall the faulty pixels automatically prior to image generation as evidenced by Rambaldi (col. 3 lines 35-38).

Re claim 4, Pape and Levine fail to teach "An image processing apparatus according to claim 1, wherein said defect correction circuit calculates an average of image data of pixels adjacent to a subject pixel". However the above limitations are well known in the art as evidenced by Rambaldi (col. 2 lines 13-15).

Therefore taking the combined teachings of Pape, Levine and Rambaldi as a whole, it would have been obvious to one skilled in the art to incorporate defect correction circuit calculates an average of image data of pixels adjacent to a subject pixel. Doing so would provide

a fault tolerant radiation imager such as a CMOS imager as evidenced by Levine(col. 2 lines 10-11).

Re claim 5, Pape and Levine fail to teach " An image processing apparatus according to claim 1, further comprising an external memory, which store position data of defective pixel of the image sensor". However the above limitations are well known in the art as evidenced by Rambaldi reads on Rambaldi. (Col. 5 lines 33-36 fig. 1).
[The reference says that it may be desirable to include memory 26 on the chip but it may be external too].

Therefore taking the combined teachings of Pape, Levine and Rambaldi as a whole, it would have been obvious to one skilled in the art to incorporate an external memory, which store position data of defective pixel of the image sensor. Doing so would provide a memory as small as possible yet large enough to store all necessary information for correction/masking for each faulty pixel as evidenced by Levine (col. 5 lines 34-36).

Re claim 6, Pape and Levine fail to teach "An image processing apparatus according to claim 1, wherein said memory is a dynamic random access memory". However the above limitations are well known in the art as evidenced by Rambaldi (col. 5 line 48).

Therefore taking the combined teachings of Pape, Levine and Rambaldi a whole, it would have been obvious to one skilled in the art to incorporate a memory, which is a dynamic random access memory. Doing so would provide a memory, which can be easily available between the size of 10 kilobits and 1 Megabit as evidenced by Levine (col. 5 lines 44-45).

Re claim 7, Pape and Levine fail to teach "An image pickup apparatus including a display device for displaying an image signal processed by the image processing apparatus according to claim 1". However the above limitations are well known in the art as evidenced by Rambaldi (col. 5 lines 25-28).

Therefore taking the combined teachings of Pape, Levine and Rambaldi as a whole, it would have been obvious to one skilled in the art to incorporate including a display device for displaying an image signal processed by the image processing apparatus. Doing so would provide for the user to visualize the corrected set of output pixels as evidenced by Levine (col. 5 lines 26-28).

[Claim 8]

An image pickup apparatus according to claim 7, wherein the display device is a liquid crystal display. Official Notice is taken of the fact that both the concept and advantages of providing a LCD as a display device are well known and expected in the art. It would have been obvious to have a LCD as a display device because it has a compact size and good image quality.

Claim 11 is a method claim corresponding to the apparatus claims 2 and 3. Therefore it has been analyzed and rejected based on the claims 2 and 3.

Claim 12 is a method claim corresponding to the apparatus claims 4. Therefore it has been analyzed and rejected based on the claim 4.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pape et al. (US Patent # 5,047,863) in view of Levine (US Patent No. 4,600,946) in further view of Hurst et al. (US Patent # 4654714).

Re claim 9, Pape and Levine fail to teach "An image processing apparatus according to claim 1, further comprising a delay circuit for delaying the image data from the image sensor by a time required for a defect correction process, if the count of said counter is not coincident with the value corresponding to the position data of the defective pixel". However the above limitations are well known in the art as evidenced by Hurst (col. 4 lines 15-20 figure 1).

Therefore taking the combined teachings of Pape, Levine and Hurst as a whole, it would have been obvious to one skilled in the art to a delay circuit for delaying the image data from the image sensor by a time required for a defect correction process, if the count of said counter is not coincident with the value corresponding to the position data of the defective pixel. Doing so would provide a FLAG signal which is timed to occur substantially synchronously with the application to defect corrector 20 of signal from recovery circuit 18 which corresponds to a response from the defective pixel as evidenced by Tabei (col. 3 lines 44-48).

6. Claims 3/2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pape et al. (US Patent # 5,047,863) in view of Levine (US Patent No. 4,600,946) in further view of Fossum (US Patent # 6611288) in further view of Rambaldi et al. (US Patent # 6618084).

Re claim 3/2, Pape, Levine and Fossum fail to teach "An image processing apparatus according to claim 2, wherein the second field of said memory stores information representative of a single defective pixel or the number of consecutive defective pixels and information

representative of a position of the defective pixel in each line". However the above limitations are well known in the art as evidenced by Rambaldi (col. 3 lines 35-38, 49-50).

Therefore taking the combined teachings of Pape, Levine, Fossum and Rambaldi as a whole, it would have been obvious to one skilled in the art to incorporate second field of said memory storing information representative of a single defective pixel or the number of consecutive defective pixels and information representative of a position of the defective pixel in each line. Doing so would recall the faulty pixels automatically prior to image generation as evidenced Rambaldi (col. 3 lines 35-38).

7. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pape et al. (US Patent # 5,047,863) in view of Levine (US Patent No. 4,600,946) in further view of Tabei (US Patent # 5805216).

Re claim 13, Pape and Levine fail to teach "An image processing method according to claim 10, wherein said step

(d) calculates an average of image data of pixels adjacent to a subject pixel in a row direction". However the above limitations are well known in the art as evidenced by Tabei (col.1 lines 63-65 figure 3A).

Therefore taking the combined teachings of Pape, Levine and Tabei as a whole, it would have been obvious to one skilled in the art to calculate an average of image data of pixels adjacent to a subject pixel in a row Direction. Doing so would provide a boundary between light

and dark portions the place X in which a defective pixel is present is conspicuous as evidenced by Tabei (col. 1 lines 17-20)

Re claim 14, Pape and Levine fail to teach "An image processing method according to claim 10, wherein said step

(d) calculates an average of image data of pixels adjacent to a subject pixel in a column direction ". However the above limitations are well known in the art as evidenced by Tabei (col. 2 line 1-2 figure 3D).

Therefore taking the combined teachings of Pape, Levine and Tabei as a whole, it would have been obvious to one skilled in the art to calculate an average of image data of pixels adjacent to a subject pixel in a column direction. Doing so would provide a boundary between light and dark portions the place X in which a defective pixel is present is conspicuous as evidenced by Tabei (col. 1 lines 17-20).

Re claim 15, Pape and Levine fail to teach "An image processing method according to claim 10, wherein said step

10 (d) performs a weighing process in accordance with distances between pixels adjacent to a subject pixel and the subject pixel". However the above limitations are well known in the art as evidenced by Tabei (col. 6 lines 46-49 figure 12A to 12L).

Therefore taking the combined teachings of Pape, Levine and Tabei as a whole, it would have been obvious to one skilled in the art to perform a weighing process in accordance with distances between pixels adjacent to a subject pixel and the subject pixel. Doing so would provide interpolation output interpolated by 12 kinds of interpolation methods as evidenced by Tabei (col. 6 lines 39-40).

Allowable Subject Matter

8. Claims 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowable subject matter:

9. As for claim 16, the prior art of record does not teach or fairly suggest the use of an image processing method, wherein the calculation process is a process of dividing a sum of pixel data of two pixels adjacent to a subject pixel and cutting a lowest one bit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K Aggarwal whose telephone number is (703) 308-9644. The examiner can normally be reached on M-F 8:00AM-4: 30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

YKA